REMARKS

The Examiner rejected claims 1 and 21-23 under 35 U.S.C. §102(b) as allegedly being anticipated by Amago et al. (US 5,402,314).

The Examiner rejected claims 5-6, 8, 10, and 24-28 under 35 U.S.C. §103(a) as allegedly being unpatentable over Amago et al. (US 5,402,314) in view of Majd (US 5,155,904).

The Examiner rejected claims 12-13 under 35 U.S.C. §103(a) as allegedly being unpatentable over Sabotke *et al.* (US 5,737,834) in view of Nakaso *et al.* (US 5,638,598), and further in view of Lauffer *et al.* (US 5,867,898).

The Examiner rejected claims 15-16 under 35 U.S.C. §103(a) as being unpatentable over Sabotke et al. (US 5,737,834)/Nakaso et al. (US 5,638,598)/Lauffer et al. (US 5,867,898) as applied to claims 12-13 above, and further in view of Majd (US 5,155,904) and Thompson, Jr. (US 5,704,535).

Applicants respectfully traverse the §102(b) and §103(a) rejections with the following arguments.

5182201858 p.12

35 U.S.C. §102(b)

SOW

The Examiner rejected claims 1 and 21-23 under 35 U.S.C. §102(b) as allegedly being anticipated by Amago *et al.* (US 5,402,314). The Examiner alleges that "Amago discloses in Fig. 12 with a solder resist 107 provided on the bottom of the PCB to obstruct molten solder."

Applicants respectfully contend that Amago does not anticipate claim 1, because Amago does not teach each and every feature of claim 1.

As a first example of why Amago does not teach each and every feature of claim 1,

Amago does not teach a first feature of: "forming a plug in the via by inserting a volume of

material into the via through the opening in the via". Applicants maintain that Fig. 12 of Amago

is nothing more than a static view of solder resist 107 on the bottom of the PCB and most

certainly does not teach said first feature of claim 1.

As a second example of why Amago does not teach each and every feature of claim 1, Amago does not teach a second feature of: "contacting an end of the plug with molten solder, wherein the end of the plug is at the bottom surface, and wherein the plug obstructs flow of the molten solder into the via". Applicants maintain that in Fig. 12 of Amago, the only structure which can be contacted by molten solder is the bottom surface of resist 107, and the bottom surface of resist 107 is below the bottom surface of the printed circuit board (PCB) and therefore is not at the bottom surface of the printed circuit board as required by claim 1.

Based on the preceding arguments, Applicants respectfully maintain that Amago does not anticipate claim 1, and that claim 1 is in condition for allowance. Since claims 3-6, 8-10, 21, and 23 depend from claim 1, Applicants contend that claims 3-6, 8-10, 21, and 23 are likewise in condition for allowance.

09/777,976

SOW p.13

35 U.S.C. §103(a)

The Examiner rejected claims 12-13 under 35 U.S.C. §103(a) as allegedly being unpatentable over Sabotke et al. (US 5,737,834) in view of Nakaso et al. (US 5,638,598), and further in view of Lauffer et al. (US 5,867,898).

The Examiner alleges: "Sabotke discloses in Fig. 1 steps of applying solder paste, reflow soldering components, and fixing a second component onto the PCB. In light of the claimed invention, Sabotke's components mounted on the top surface will be the bottom components mounted in the claimed invention, and vice versa. Sabotke fails to disclose providing a PCB having a soldered via electrically communicating between layers as well as top to bottom layers and screen printing solder. Nakaso discloses in Fig. 3 a solder plug in a via formed in a PCB. Lauffer discloses in claim 8 screening the solder paste. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sabotke by providing a PCB having a soldered via electrically communicating between layers as well as top to bottom layers and screen printing solder, as taught by Nakaso and Lauffer, for the purpose of allowing forming densenly formed contacts to electrically communicate between layers and top and bottom surfaces, as well as increase production by mass soldering a plurality of vias and pads."

Applicants respectfully contend that claim 12 is not unpatentable over Sabotke in view of Nakaso, and further in view of Lauffer because it is not obvious to modify Sabotke with Lauffer's solder paste screening steps and Nakaso's solder plug.

A first reason why the preceding combination of references is improper is that forming a via in Sabotke's PCB is irrelevant to Sabotke's invention. Sabotke invention relates only to the efficiency of installing components on the top and bottom surfaces of a PCB and is totally

09/777,976

unconcerned with electrical communication between the components on the top surface and the components on the bottom surface. Applicants maintain that forming a via in Sabotke's PCB would in no way improve the invention that Sabotke discloses.

A second reason why the preceding combination of references is improper is that, even if it is obvious to form a via in Sabotke's PCB (which it isn't), it is not obvious to plug the via with a solder plug to satisfy the Examiner's stated reason of "allowing forming densenly formed contacts to electrically communicate between layers and top and bottom surfaces". All that is required to satisfy the Examiner's stated reason is to have an electrically conductive material in the via continuously extending between the top and bottom surfaces of the PCB. It is irrelevant to the Examiner's stated reason for said electrically conductive material to function as a plug in the via. Indeed, having said electrically conductive material function as a plug will require more material and add unnecessary weight. In any event, Applicants maintain that it is not obvious for the said electrically conductive material to function as a plug in the via.

A third reason why the preceding combination of references is improper is that it is not obvious to form and plug the vias with a solder plug to satisfy the Examiner's stated reason of "increas[ing] production by mass soldering a plurality of vias and pads". Applicants contend that production by mass soldering will not be increased by forming plugs within the vias as compare to not forming plugs within the vias. Therefore, Applicants maintain that it is not obvious to form a plug in the via.

Additionally, Applicants respectfully maintain that the Examiner's argument with respect to Nakaso is an improper modification of the secondary reference of Lauffer. The Examiner

09/777,976

argues that the primary reference of Sabotke discloses "applying solder paste, reflow soldering components, and fixing a second component onto the PCB". The Examiner also argues that the secondary reference of Lauffer has modified the primary reference of Sabotke, by alleging that Lauffer teaches or suggests having a via in Sabotke's PCB and screning solder paste in said via. The Examiner additionally argues that the secondary reference of Nakaso has modified the secondary reference of Lauffer, by alleging that Nakaso teaches or suggests having the solder paste screened according to Lauffer form a sold plug in the via. Applicants maintain that it is improper to argue that a claim feature is taught or suggested by a secondary reference through modification of another secondary reference. If the Examiner could modify a secondary reference in the preceding manner, then the Examiner would be able to show the existence of any element or feature of any claim merely by chaining a sufficient number of secondary references together in the preceding manner. Accordingly, Applicants respectfully maintain that the rejection of claim 12 under 35 U.S.C. §103(a) is improper and should be withdrawn.

Based on the preceding arguments, Applicants respectfully maintain that claim 12 is not unpatentable over Sabotke in view of Nakaso, and further in view of Lauffer, and that claim 12 is in condition for allowance. Since claims 13, 15-16, 22, and 24-28 depends from claim 12, Applicants contend that claims 13, 15-16, 22, and 24-28 are likewise in condition for allowance.



CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invites the Examiner to contact Applicants' representative at the telephone number listed below.

Date: 09/08/2003

Jack P. Friedman Registration No. 44,688

Schmeiser, Olsen & Watts 3 Lear Jet Lane, Suite 201 Latham, New York 12110

(518) 220-1850

RECEIVED CENTRAL FAX CENTER SEP 0 8 2003

09/777,976

OFFICIAL